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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/705,696	11/06/2000	Joonbae Park	GCT-011	7786

34610 7590 04/05/2005

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EXAMINER	
BAYARD, EMMANUEL	
ART UNIT	**PAPER NUMBER**
2631	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/705,696	PARK ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is in response to amendment after final filed 3/17/05 in which claims 1-30 are pending. The final rejection dated 11/17/04 has been withdrawn. In addition applicant's arguments and amendment have been considered and entered but they are moot based on the new ground of rejection. Therefore this case is made final.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al U.S. patent No 6,516,187 B1 in view of Hagerty U.S. Patent No 5,371,479.

As per claims 1 and 7, Wiiliams et al teaches a loop apparatus, comprising: a plurality of gain stages connected in series to amplify a radio frequency (RF) signal having a voltage, wherein each gain stage includes an input port that receives the signal and an output port that transmits the resulting amplified signal (see fig.2 elements 210-216 and col.3, lines 22-40) and each stage increases the voltage of the RF signal; a feedback loop (see fig.2 element 218 and col.3, lines 34-40) that cancel an undesired offset of the resulting amplified signal wherein feedback loop connects to the output port and the input port (see abstract).

However Williams et al does not teach a plurality of feedback loops wherein each feedback loop connects to the output port and the input port of a corresponding one of the gain stages, such that each gain stage is connected to a corresponding feedback loop that cancels the undesired offset) (see figs. 4-6) of its corresponding gain stage.

Hagerty teaches a plurality of feedback loops (see fig.1 elements 140, 240, 319, 373 and col.2, lines 16-55 and col.3, lines 28, 53 and col.4, lines 19-60) wherein each feedback loop connects to the output port and the input port of a corresponding one of the gain stages, such that each gain stage is connected to a corresponding feedback loop that cancels the undesired offset (see col.5, lines 10-15, 40-45) of its corresponding gain stage.

It would have been obvious to one of ordinary skill in the art to implement the teaching of Hagerty into Williams as to obtain high gain and accurate transient response around the stage loops as taught by Hagerty (see col.5, lines 38-43).

As per claim 2, Williams et al includes a direct current offset voltage correction (see abstract).

As per claim 3, Williams et al includes a high-pass filter that filters the direct current offset voltage (see col.1, line 32).

As per claim 4, Williams et al includes a variable gain amplifier (see fig.2 element 201).

As per claim 5, Williams et al includes a capacitor (see fig. 3 element 320), and feedback loops mounted on a Chip (see col.3, lines 3-5).

As per claim 6, Williams et al includes an analog radio frequency signal (see col.1, line 7).

As per claims 17 and 21, Williams et al includes an analog amplified signal (see col.1, line 7).

As per claims 20 and 24, Williams et al and Hagerty in combination would teach a loop apparatus within a single amplification unit as to obtain high gain and accurate transient response around the each stage loop as taught by Hagerty (see col.5, lines 38-43).

As per claims 26-30 Williams et al and Hagerty in combination would teach an antenna unit to provide the RF signal to at least a first one of the gain stages as to accurately detect the signal sampling during the receiving process.

As per claim 8 Williams et al a direct conversion receiver, comprising: an amplification unit that receives and amplifies a RF signal (see fig.2), wherein the amplification unit includes a plurality of gain stages connected in series to amplify a radio frequency (RF) signal having a voltage, wherein each gain stage includes an input port that receives the signal and an output port that transmits the resulting amplified signal (see fig.2 elements 210-216 and col.3, lines 22-40) and each stage increases the voltage of the RF signal; a feedback loop (see fig.2 element 218 and col.3, lines 34-40) that cancel an undesired offset of the resulting amplified signal wherein feedback loop connects to the output port and the input port (see abstract); a mixer that demodulates the amplified signal by mixing (see fig.2 element 240 or 260) the amplified RF signal

with a local oscillation (see fig.2 element 202 and col.3, lines 60-67 and col.4, lines 1-3) signal to form a base band signal.

However Williams et al does not teach a plurality of feedback loops wherein each feedback loop connects to the output port and the input port of a corresponding one of the gain stages, such that each gain stage is connected to a corresponding feedback loop that cancels the undesired offset) (see figs. 4-6) of its corresponding gain stage.

Hagerty teaches a plurality of feedback loops (see fig.1 elements 140, 240, 319, 373 and col.2, lines 16-55 and col.3, lines 28, 53 and col.4, lines 19-60) wherein each feedback loop connects to the output port and the input port of a corresponding one of the gain stages, such that each gain stage is connected to a corresponding feedback loop that cancels the undesired offset (see col.5, lines 10-15, 40-45) of its corresponding gain stage.

It would have been obvious to one of ordinary skill in the art to implement the teaching of Hagerty into Williams as to obtain high gain and accurate transient response around the stage loops as taught by Hagerty (see col.5, lines 38-43).

As per claims 9, 19, 23, Williams and Hagerty in combination would teach an analog-to digital converter as to sample the IF demodulated base band signal to a digital sampling data stream.

As per claim 10, Williams includes a channel selection filter (see col.3, line 12). Furthermore implementing such teaching for removing an out-of-band signal from the

demodulated base band signal would have been obvious to one skilled in the art as to a noiseless and accurate IF demodulated signal.

As per claim 11, Williams and Hagerty in combination would include a direct current offset voltage and each feedback loop includes to cancel an undesired offset of the resulting amplified signal direct current offset canceling unit for rejecting the direct current offset voltage accumulated by its corresponding gain stage as to determine a degree of similarly between the input signal and the output signal.

As per claim 12, Williams et al teaches a high-pass filter that filters the direct current offset voltage (see col.1, line 32).

As per claim 13, Williams et al teaches a variable gain amplifier signal (see fig.2 element 201).

As per claim 14, Williams et al includes a capacitor (see fig. 3 element 320), and feedback loops mounted on a Chip (see col.3, lines 3-5).

As per claims 15 and 25, Williams et al includes an analog amplified signal (see col.1, line 7).

As per claim 16, the local oscillator signal of Williams et al would generate a plurality of clock signals, wherein each of the clock signals has a frequency less than the local oscillator signal as to accurately recover the input timing signal during the operation.

As per claims 18-19 and 22 Williams et al a mixer that demodulates the amplified signal by mixing (see fig.2 element 240 or 260) the amplified RF signal with a

local oscillation (see fig.2 element 202 and col.3, lines 60-67 and col.4, lines 1-3) signal to form a base band signal.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
Primary Examiner
Art Unit 2631

EMMANUEL BAYARD
PRIMARY EXAMINER